REMARKS

The present application was filed on November 21, 2003 with claims 1-20. Claims 1-20 are currently pending in the application. Claims 1, 19 and 20 are the independent claims.

In the Office Action, claims 1, 3, 4, 6-8, 10-13, 18 and 19 are rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,969,538 (hereinafter "Whetsel") in view of allegedly admitted prior art involving FIG. 2 of the present application. In addition, claims 17 and 20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Whetsel in view of allegedly admitted prior art of FIG. 2 in further view of U.S. Patent No. 6,681,352 (hereinafter "Fredrickson").

The Examiner indicates that claims 2, 5, 9 and 14-16 would be allowable if rewritten in independent form.

Applicants respectfully traverse the §103(a) rejections of claims 1, 3, 4, 6-8, 10-13 and 17-20. Applicants respectfully request reconsideration of these claims in view of the following remarks.

Applicants initially note that for a valid §103(a) rejection, the reference or reference combination must teach or suggest all the claim limitations. Manual of Patent Examining Procedure (MPEP), Eighth Edition, August 2001, §2143. In addition, an obviousness rejection based on a combination of references must show "some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings." Id.

Claim 1 sets forth:

> An apparatus comprising:
>
> an integrated circuit die comprising an internal signal pad arranged at a location away from a periphery of the die, a peripheral signal pad arranged proximate the periphery of the die, and a switch coupled between the internal signal pad and the peripheral signal pad;
>
> the switch being configurable in at least a first state in which the internal signal pad is not operatively connected to the peripheral signal pad, and a second state in which the internal signal pad is operatively connected to the peripheral signal pad;
>
> the switch being configurable in one of the first and second states responsive to a control signal having one of first and second signal characteristics, respectively;
>
> wherein the switch is configured in the first state during normal operation of the integrated circuit die; and

wherein the switch is configured in the second state to permit test access to the internal signal pad via the peripheral signal pad.

Advantageously, an illustrative embodiment in accordance with claim 1 allows efficient test access to these internal analog signal pads in an integrated circuit without the excessive cost and other difficulties associated with use of a membrane probe card, and without degrading analog signal performance during normal operation of the corresponding packaged integrated circuit (Specification, p. 4, lines 3-6).

In formulating the §103(a) rejection of independent claim 1, the Examiner argues that the Whetsel-FIG. 2 reference combination teaches or suggests "a switch coupled between the internal signal pad and the peripheral signal pad" (Office Action, pp. 2-3). Applicants respectfully disagree. Whetsel only teaches the use of peripheral signal pads. See, e.g., Whetsel, FIGS. 1, 4, 5 and 6. Therefore, while Whetsel teaches an apparatus that can connect two peripheral signal pads by a series of switches, Whetsel, unlike claim 1, fails entirely to teach or suggest a switch that couples internal signal pads to peripheral signal pads. Moreover, FIG. 2 fails to correct this deficiency in Whetsel. Therefore, the Whetsel-FIG. 2 combination fails to teach or suggest one or more limitations of claim 1.

In addition, Applicants respectfully assert that Whetsel and FIG. 2 are devoid of any suggestion or motivation that would cause one skilled in the art to combine the references in the way suggested by the Examiner. To the contrary, both Whetsel and FIG. 2 teach away from the combination proposed by the Examiner. "A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant." In re Gurley, 27 F.3d 551, 553, 31 USPQ2d 1130 (Fed. Cir. 1994).

As stated above, for example, Whetsel only teaches the use of peripheral signal pads to test the internal core logic circuitry of an integrated circuit. This allows the integrated circuit to be tested using a conventional pad probe assembly that makes contact to only peripheral signal pads (Whetsel, FIG. 4 and col. 2, lines 25-28). One skilled in the art, therefore, upon reading Whetsel, would be led to use only peripheral signal pads when testing an integrated circuit.

Moreover, with respect to FIG. 2, the specification states at p. 1, line 28 through p. 2, line 5:

> A problem associated with use of area array buffers such as those shown in FIG. 2 is that it is difficult to gain access to internal analog signal pads during testing that occurs before the integrated circuit die is packaged. Such pre-package testing typically involves testing the integrated circuit die while it is still part of the semiconductor wafer, that is, before the wafer is cut into chips which are individually packaged, and is thus also referred to herein as wafer-level testing. The wafer-level testing is carried out using a wire-type wafer probe card comprising many short but stiff wires, referred to as test probes, that temporarily connect the peripheral bonding pads of the integrated circuit die to an associated test apparatus.

In addition, the specification further states at p. 2, lines 12-20:

> Although there is another type of wafer probe card, known as a membrane probe card, which can reach internal bonding pads within an area array during wafer-level testing, this type of card is generally very expensive and difficult to use.
>
> One possible alternative is provide permanent connections between the bonding pads inside the area array to corresponding peripheral bonding pads for wafer-level testing. However, this approach is usually appropriate only for digital signal pads, since for analog signal pads the connecting wires may add unacceptable amounts of parasitic resistance and capacitance, thereby degrading analog signal performance during normal operation of the subsequently-packaged integrated circuit.

Therefore, the specification clearly sets forth that using the FIG. 2 arrangement presents a problem with gaining test access to the internal signal pads, and that the solutions available in the prior art are either expensive and difficult to use, or appropriate only for certain types of signal pads. Undoubtedly, therefore, one skilled in the art, upon reading this text in association with FIG. 2, would be discouraged from using internal signal pads.

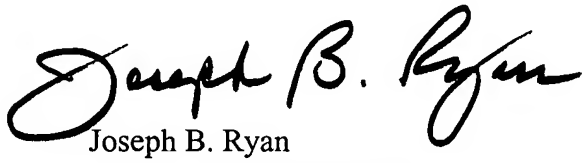
For the foregoing reasons, Applicants respectfully submit that claim 1 would not have been obvious at the time the invention was made in view of the Whetsel-FIG. 2 combination. Independent claim 19 contains analogous limitations to claim 1. Therefore, Applicants also submit that this independent claim should be allowed for reasons similar to those stated above for claim 1.

Dependent claims 3, 4, 6-8, 10-13 and 18 are believed to be in condition for allowance for at least the same reasons as their respective independent claims.

With respect to the §103(a) rejection of claims 17 and 20 over Whetsel in view of FIG. 2 in further view of Fredrickson, Applicants note that Fredrickson does not correct the fundamental deficiencies of Whetsel and FIG. 2, as described above. Therefore, claims 17 and 20 would also not have been obvious at the time the invention was made.

In view of the above, Applicants believe that claims 1-20 are in condition for allowance, and respectfully request the withdrawal of the §103(a) rejections.

Respectfully submitted,



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